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A Semiconductor Nano-Patterning Approach Using AFM-Scratching Through Oxide Thin Layers

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ABSTRACT

AFM-scratching was performed through thin oxide layer which was either a native oxide layer (1.5 – 2 nm thick) or a thermal oxide layer (10 nm thick). Due to their insulating properties, the SiO_2 films act as masks for the metal electrochemical deposition. In the scratched openings copper deposition can take place selectively and thus nano-scale metal lines could be successfully plated onto the p-type silicon substrates. Using particularly, if sufficiently thick thermal oxide has advantages over the native oxide, it allows a H-termination of the Si within the grooves (HF treatment) without eliminating the oxide layer on the rest of the surface.

INTRODUCTION

Since the recent incorporation of electrodeposited copper into electronic devices, a renewal of interest for electrodeposition and related technologies have found new applications in electronics manufacturing, especially for packaging and magnetic recording [1]. Usually photolithography is used in industrial processes to pattern surfaces in the micrometer range. However miniaturization and the promising properties of nano-scaled materials ("quantum confinement") have stimulated research groups to explore alternative patterning techniques. Most of these structuring methods are based on lithography requesting therefore a masking process. Based on this principle high resolution patterning can be performed using electron-beam, x-rays, or scanning probe microscopies to sensitized the resist layer (see e.g., Ref. [2-4]). The other approaches consist of direct selective reactions at the semiconductor surfaces. Different techniques are proposed such as pre-sensitization of the surface by focused ion beam followed by selective electrochemical deposition or dissolution at the implanted locations [5,6]. Another example is the use of an electrochemical-scanning tunneling microscope (EC-STM) to deposit nanometer scaled metallic clusters onto metal and semiconductor surfaces [7]. Under the scanning of the optical tip of a scanning near-field optical microscope (SNOM), it is also possible to use the light to generate and control the local photocurrent that triggers the electrochemical reactions at the scanned locations with a high lateral resolution [8]. Other techniques are reported in literature and a review of these techniques is proposed in Ref. [9]. In a previous paper, an atomic force microscope (AFM) was used to created nano-scratches onto silicon surface covered by the native oxide layer. Due to the masking properties of this oxide film, it was possible to selectively deposit copper within the grooves with a sub-micrometer

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lateral resolution [10,11]. The present work investigates the use of this AFM-scratching method through a thin thermal oxide layer to optimize the process.

EXPERIMENTAL

Experiments were carried out on p-Si (100) wafers (1 to 10 Ω·cm) that were thermally oxidized (thickness 10 nm). Samples were degreased by subsequently sonicating in acetone, isopropanol, methanol and rinsed with distilled water. The back contact to the Si electrodes was established by smearing InGa eutectic (99.99%). The electrochemical cell consisted of three-electrodes configuration with Pt gauze as counter electrode and a Haber-Luggin capillary with a Ag/AgCl electrode as reference electrode. The electrochemical deposition was performed in 0.01 M CuSO4 + 0.05 M H_2SO_4 using a Jaissle 1002 T-NC potentiostat. The electrochemical cell was placed in a black box in order to avoid non-controlled photo-electrochemical effects. AFM scratching and imaging were carried out using a PicoSPM microscope from Molecular Imaging driven by a Nanoscope E controller from Digital Instruments. The device was equipped with a three-sided pyramidal single-crystalline diamond tip provided by Digital Instruments (more details about the procedure can be find in Ref. [10]). Chemical analysis was performed by Auger electron spectroscopy (AES) using a Physical Electronics PHI 670. During these experiments, the probe was scanned, line by line, over the sample in the perpendicular direction of the scratches, monitoring the Si LMM signal at 1621 eV and Cu LMM at 922 eV. X-ray photoelectron spectroscopy (XPS) was used to determine the thickness of the silicon dioxide layer after different etching times in HF 1%. The XPS analyzer was a Physical Electronics PHI 5600 series instrument with a monochromatic Al K_α x-ray source. The Si 2p peaks at 99.5 and 104 eV were monitored during the Ar^+ sputtering. Ellipsometric measurements of the oxide film thickness were performed with a Sentech Instruments SE 800 spectrometric ellipsometer equipped with a Xe lamp. Scanning electron microscope (SEM) images were acquired with a JEOL 6400 equipped with tungsten filament.

RESULTS AND DISCUSSION

Figure 1a shows an AFM image of a series of scratches carried out at a constant normal applied force (50 μN) for various number of cycles (N = 10, 20,30,40, 50, 60) on oxide-covered silicon. The scratches are well defined and little debris is visible because the abraded particles are swept out of the observation window by the tip. The protrusions along the sides of the scratches result of surface deformation induced by the mechanical treatment and indicate the presence of stress. The cross section, presented in Figure 1b, gives information about the scratch geometry. The grooves have a V-shape and as expected the scratch size increases with N : between 14 nm to 38 nm in depth and between 183 nm to 265 nm in width. In a previous work [10], the influence of the load on the scratch morphology has been investigated. From those experiments, obtained on native oxide layer-covered silicon wafers, it is apparent that the scratch sizes increase linearly with the normal applied force. The plastic deformation threshold was estimated to be near 14 μN.

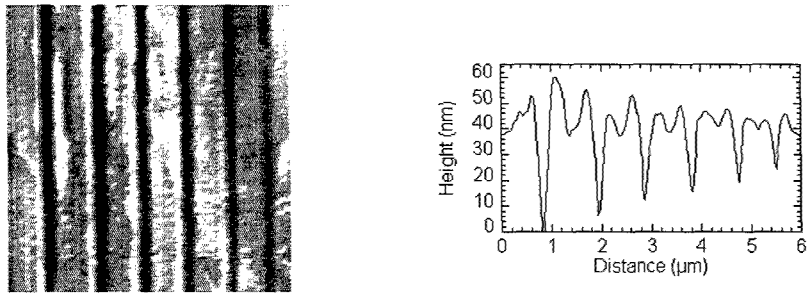

Figure 1: (a) AFM top view of a scratched Si surface (6×6 μm). The 6 AFM-scratches are 20 μm long. Number of cycle varies from left to right: 60, 50, 40, 30, 20, 10. Normal applied force is 50 μN, scan rate is 40 μm/s. (b) Cross section of the top view presented in (a). From Ref. [12].

It was shown before [10] that AFM scratches performed onto p-Si are activated locations for electrochemical deposition. However undesired deposition near the scratches was observed and the sample preparation method was therefore modified. The H-termination of the Si surface by dip in HF 1% was eliminated and thus the native oxide layer present on the Si was not dissolved. In this case, AFM-scratching was carried out through the native oxide layer into the semiconductor substrate. After scratching, the samples were transferred as quickly as possible to the electrochemical cell in order to minimize the regrowth of the oxide layer within the scratches and thus to create two zones on the silicon surface, one "passivated" by the native oxide layer and one "activated" (Si surface within AFM-scratches). Figure 2 shows copper deposit performed at – 500 mV (vs. Ag/AgCl) during 1 s for native oxide layer covered samples. It is clear that highly selective metal deposition is obtained for this type of samples. Copper deposition occurs only at the scratch locations and no copper clusters are observable on the intact surface.

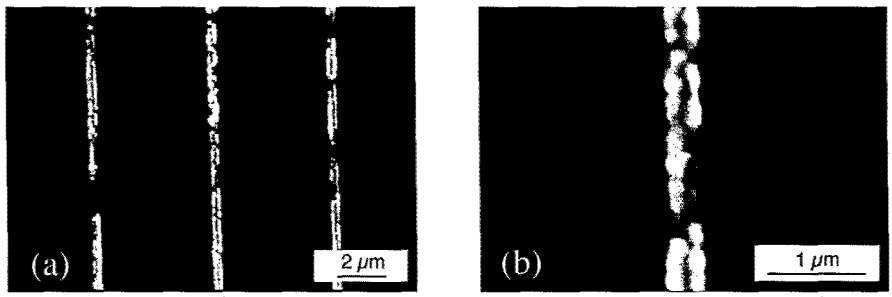

Figure 2: SEM images of Cu lines deposited on AFM scratches produced in a native oxide layer covered p-Si surface. The scratches were made with a force of 15 μN. Deposition was carried out from 0.01 M $CuSO_4$ + 0.05 M H_2SO_4 electrolyte applying a potential step to – 500 mV (vs. Ag/AgCl) during 1 s. (b) Higher magnification of a Cu line presented in (a).

As the deposition time was short (1 s) these images provide information about the initial step of the copper growth. These images show that deposition is initiated on the scratch edges. At

short deposition times, there are two copper lines apparent on one scratch. It was observed that for longer deposition time coalescence of the two lines into a single Cu line occurs. For longer deposition times, copper overgrowth of the insulating native oxide layer can occur. The crystallite morphology suggests that initiation and growth of the 3D metal (Me) phase follows the Volmer-Weber or island growth mechanism. This is in line with the observation of generally weak Me_{ads}-Semiconductor interactions [13].

Native oxide reformation in the scratches appeared to be a possible limiting factor to achieve homogeneous metallic lines especially for short deposition time. Thus an optimization of the process was investigated. A thin oxide layer with a thickness of 10 nm was thermally grown in order to authorize a H-termination of the Si within the grooves by dipping the wafer in HF 1% just after the AFM-scratching step. Note that by this techniques, it was possible to store the scratched sample as the air-formed oxide is surely dissolve just before the electrochemical step. This process is described in Figure 3.

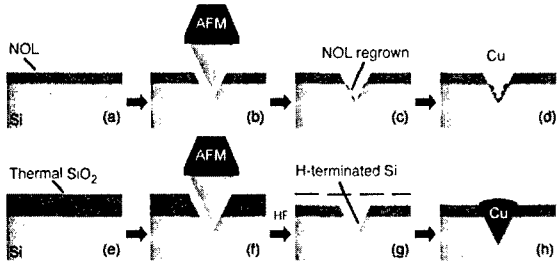

Figure 3: Schematic of the approaches for selective electrochemical deposition of metal within AFM-scratches. First process: (a) Si covered by the native oxide layer (~2 nm), (b) AFM-scratching through the native oxide layer, (c) oxide regrowth within the scratch, (d) selective electrochemical deposition of Me within the scratches hampered by the reform oxide. Second process: (e) Si covered by a dry oxide (10 nm), (f) AFM-scratching through the oxide layer, (g) removal of the native oxide regrown in the scratch and H-passivation, (h) selective electrochemical deposition of Me within the scratch.

The etching rate of the oxide was studied in order to optimize the HF (1%) dip duration. The film thickness measured by XPS and ellipsometry after the immersion of the oxide-covered sample in HF (1%) for different times. An etching time of 30 s was found to be the adequate time. Approximately 4 nm of the thermal oxide layer are removed leaving a 6 nm thick oxide film on the surface while the native oxide layer within the scratches is fully removed, and there, the Si is H-terminated. Additional experiments performed on native oxide covered wafers have confirmed that the dissolution rate of the two types of oxides is similar. Preliminary experiments were carried out on oxide-covered samples scratched with a micro-indentor equipped with a diamond tip for Vickers test. The normal applied load was 49 mN creating scratches of 3 µm in width and 300 nm in depth. Potential step deposition performed at – 500 mV during 10 s are shown in Figure 4.

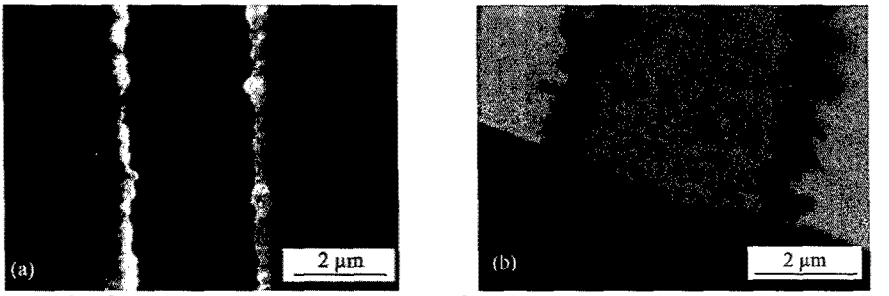

Figure 4: SEM top view (a) and cross section (b) of Cu deposits on oxide covered p-Si scratched with a micro-indentor with a normal applied force of 49 mN. Cathodic potential steps carried out in $CuSO_4$ (0.01 M) + H_2SO_4 (0.05M) at – 500 mV for 10 s.

These SEM pictures confirm the considerable role of the scratch edges during the nucleation phase. On these larger scratches the deposit is exclusively located on each sides of the grooves and only few crystallites are observed within the scratches. It seems that either the Si/SiO_2 interface is an activating location for copper nucleation or the oxide layer is deteriorated by the scratching process in the vicinity of the groove allowing deposition at these sites. In both cases a high defect concentration seemed to activate the metal deposition. At smaller scale (AFM scratching) this effect is less visible due to the earlier coalescence of the metallic lines.

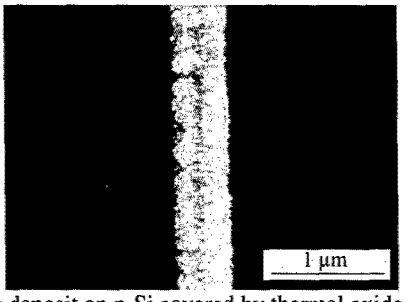

Figure 5: SEM image of Cu deposit on p-Si covered by thermal oxide. Cathodic potential steps carried out in $CuSO_4$ (0.01 M) + H_2SO_4 (0.05M) at – 500 mV for 10 s.

Deposition on thermal oxide covered p-Si is presented in Figure 5. The homogenous Cu line is smaller than in the case of the native oxide covered sample. On the thermal oxide covered silicon it was possible to reach smaller Cu line dimension (480 nm). It can be explained by several factors. In this case, indeed, the Si surface in the scratch is fully H-terminated and therefore the oxide regrowth is prevented and due to the higher thickness of the oxide film, the active size of the groove is smaller than the one for native oxide covered sample. The copper is then more confined in the groove, metal overgrowth is limited and homogeneity is better.

AES mapping for Cu obtained on Cu lines deposited on oxide-covered p-Si has confirmed that the deposition takes place with a very high degree of selectivity. No Cu is detected outside the scratched location. Even when a $\approx 16\ \mu m^2$ square area situated between two copper lines was

analyzed with high integration time, the presence of copper could not be detected. This demonstrates that metal deposition occurs only in the AFM-scratches.

CONCLUSION

The work clearly shows that a thin oxide layers can efficiently be used for masking metal deposition on p-type Si. Scratches produced through this oxide layers using an AFM can be used to open "activated" patterns on the Si surfaces. Onto these patterns metal electrodeposition can be performed selectively, and hence can be used for semiconductor patterning and functionalization by selective electrodeposition in the sub-micrometer range. From the results presented here, it appears clearly that using a thin thermal oxide film as mask, a higher resolution and particularly a better homogeneity can be reached. Copper nucleation is initiated at the groove edges indicating either a high degree of reactivity of the Si/SiO_2 interface or that the oxide layer is deteriorated by the scratching at these locations. This technique should essentially be applicable to any material that can be electrochemically deposited and thus bears the potential to create nano-patterns of a large palette of materials.

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